Engineering considerations in design of high temperature electronics for planetary probes

R. Frampton[1] ; L. Peltz[1], S. Rubin[1], T. Hussain[2], T. Andrews[1]

1 – The Boeing Company
2 – Hughes Research Laboratories

6th International Planetary Probe Workshop, 2008
Wednesday, June 25, 2008
Atlanta, Georgia

The Challenge for the Entry Phase in the Mission

PRIMARY TECHNICAL CONSTRAINT:

1. Properties of binding materials – cannot exceed 260^{o} C.
2. Minimize Thickness and weight of the TPS material – but meet 260^{o} C constraint
3. Thus electronics, to be embedded in TPS, must be qualified to 260^{o} C.

TRADE-OFF PARAMETERS:

1. Thickness of material
2. Heating rates
3. Electronics technologies

Illustrative Example ~ Properties for Orion:

Lunar direct return conditions:

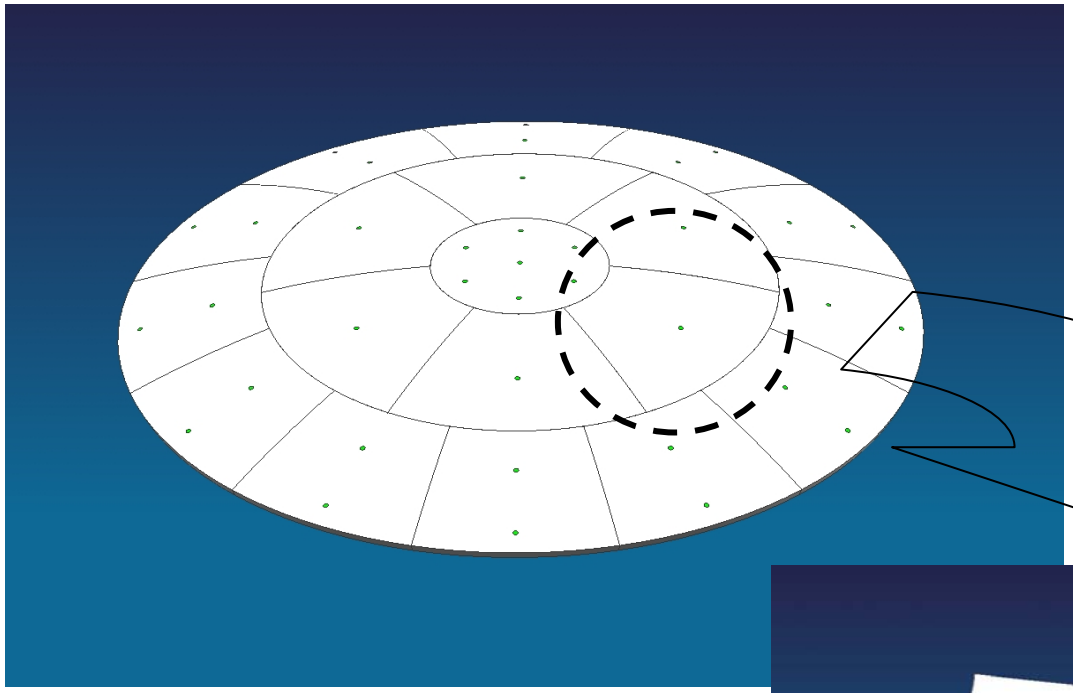
- **11 km/s atmospheric entry**
- **peak heat rate > 750 W/cm^2**

LEO return conditions:

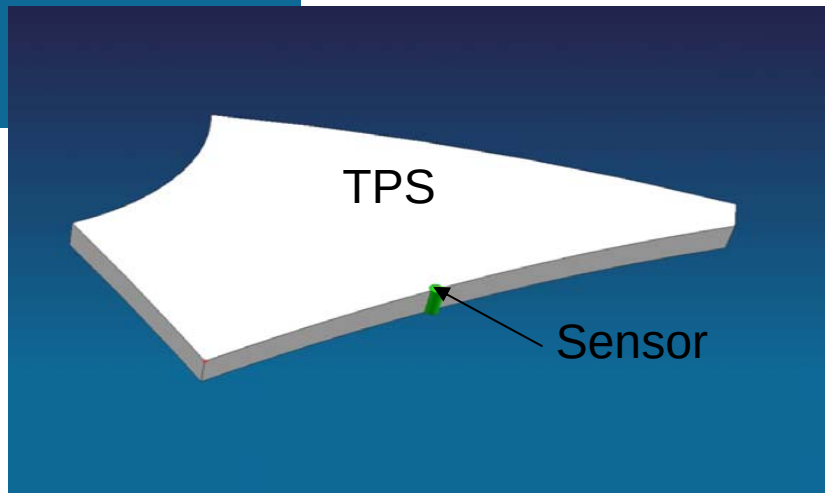
- **8 km/s atmospheric entry**
- **peak heat rate > 100 W/cm^2**

Galileo Probe

Heat Shield Sensors



Multiple sensor modules would be embedded into an instrumented TPS material as implemented in Galileo, Orion, etc..



CEV Heat Shield Sensor Architecture for Extreme Environments

Background (the technical problem to be solved):

The TPS and heat shield will be generously instrumented during the atmospheric entry. Sensors could include, for example, 100 thermal couples, 50 recession sensors, 20 pressure sensors, and accelerometers. These sensors will require electronic circuits for interface and data collection. At locations behind the PICA TPS, the temperatures may reach, in worst-case conditions, up to 260º C = 500º F.

Background (A feasible technology):

Silicon Germanium (SiGe) Electronics for Extreme Cryo Environments is being developed under NASA RHESE program managed by Dr. Andrew Keys, MSFC.

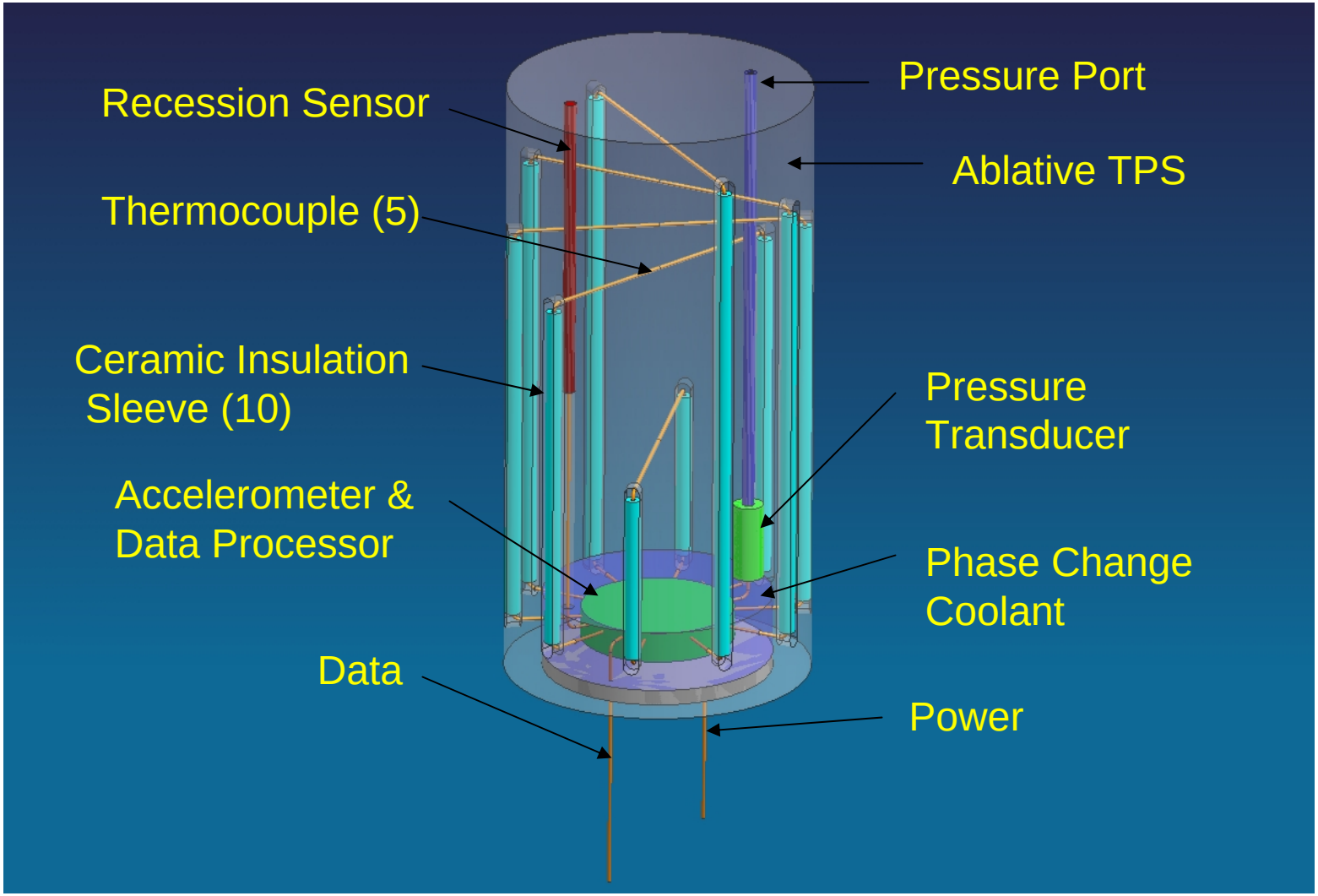
NASA program for SiGe Electronics for Extreme Environments performed by multi-disciplinary team (university, industry, NASA) led by Prof. John Cressler at Georgia Tech.

SiGe technology is currently being tested under Boeing IRAD to demonstrate its ability to operate at high temperatures.

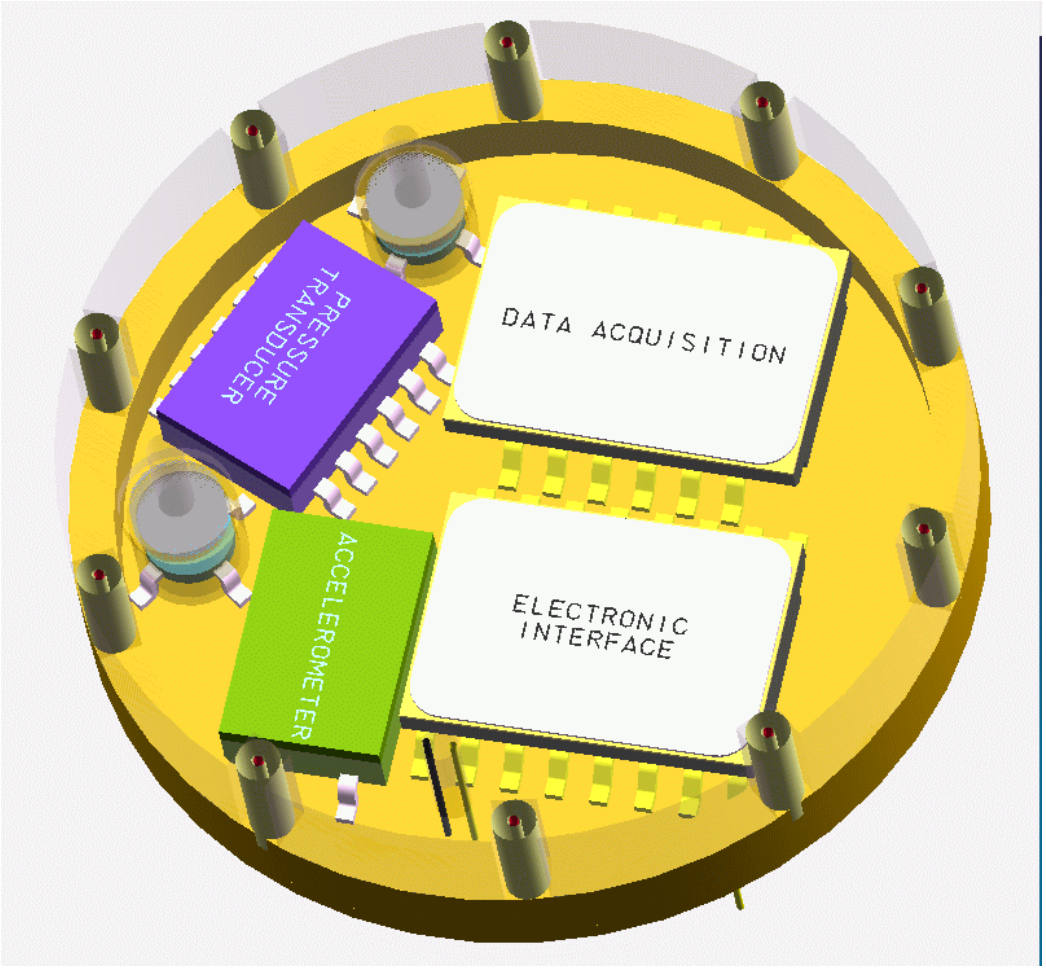
SiGe HBT devices also have intrinsic tolerance to radiation, as demonstrated in tests with multi-MRad total dose.

... by implementing integrated sensor measurement architecture using SiGe electronic modules, to operate without failure up to 260º C (500º F).

Heat Shield Sensor Module



SiGe Electronics Embedded in TPS Sensor Module

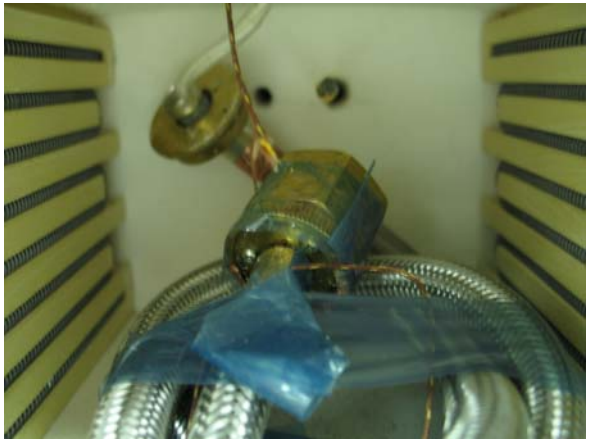


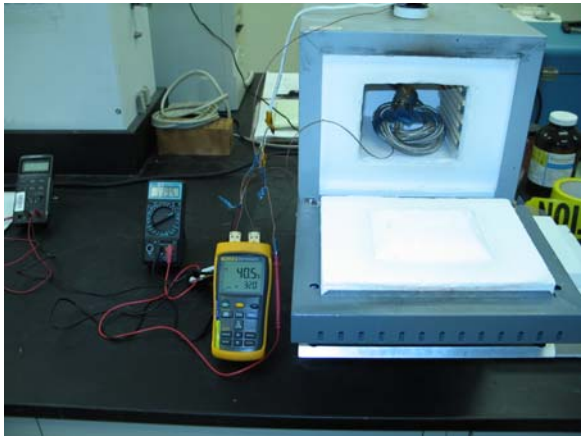
TECHNICAL APPROACH FOR VALIDATION OF INSTRUMENTED Heat Shield Sensor Architecture for Extreme Environments

Technical Approach to Our Test Program:

1. Test a representative SiGe circuit in oven tests, for validation of performance at high temperatures, to 260^{o} C.
2. Provide customized high temperature packaging for operation in the very high electronic noise inherent to an arc jet test site (this electric noise is not encountered behind a typical TPS structure during reentry). Test the same SiGe circuit, in a custom designed package for environment of high acoustic noise, behind the TPS panels.
3. Design alternative (backup) package that incorporate phase-change materials, for demonstration of feasibility of additional margin.
4. Test and demonstrate the representative SiGe circuit during arc jet tests. The SiGe electronics is powered and operational while embedded in the back of the PICA coupon during the arc jet test, in the environment where temperatures may reach 260^{o} C (500^{o} F).

Testing Si Ge at high temperature, using the oven in the lab

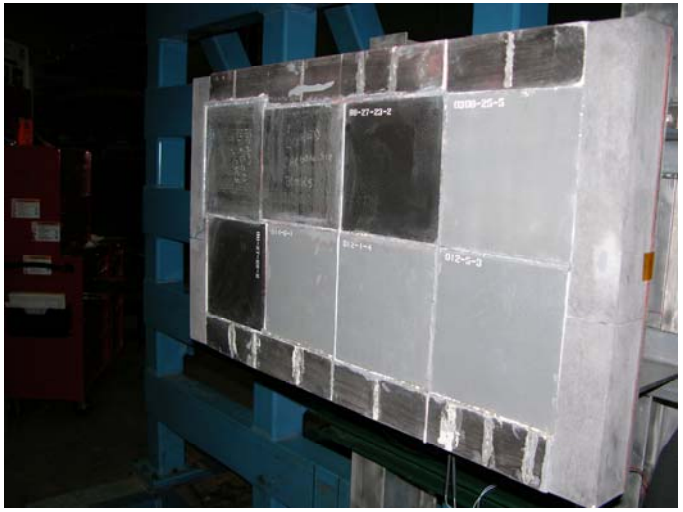




Experimental setup in the Boeing Instrumental Analysis Lab

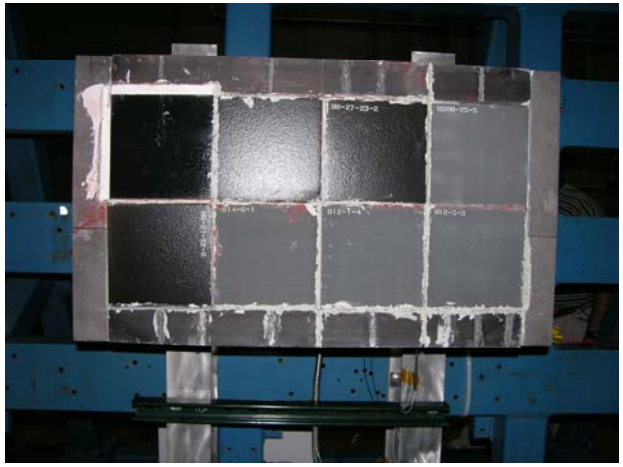
Testing of SiGe Electronics at high temperatures

1. Tests up to 200º C, on unpackaged die, performed by Boeing together with the group of Prof John Cressler at Georgia Tech.
   Tests completed successfully, no evidence of functional degradation of electronics.
2. Acoustic and high-temp tests performed by Boeing at AFRL Dayton, on packaged SiGe circuit, housed within a module. Module located behind TPS (tiles) panel. TPS panel subjected to acoustic noise and front temperatures up to 2300º F.
   Tests completed successfully, no evidence of functional degradation of electronics.



TPS (tile) panel being tested at AFRL

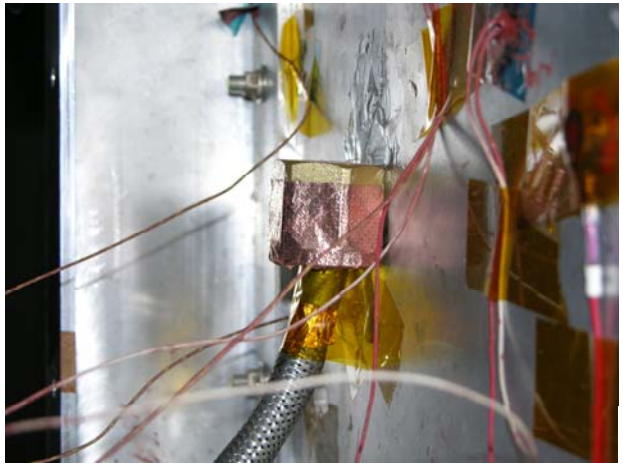
Testing of SiGe Electronics at high temperatures at AFRL



TPS (tile) panel – front side in rack

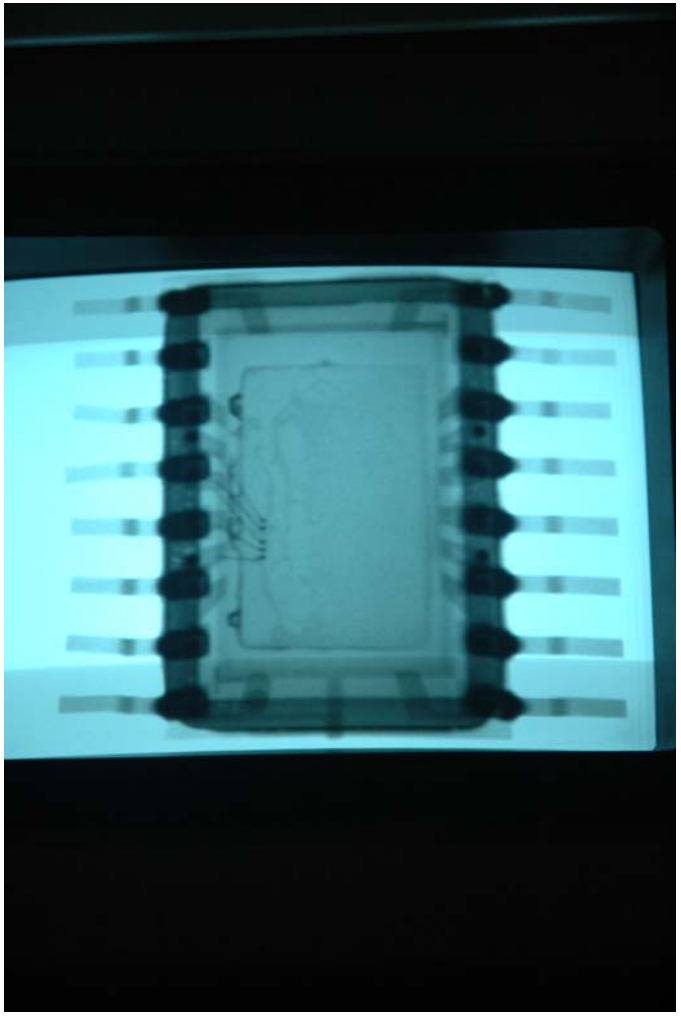
Back side of panel, showing SiGe module and the Boeing test monitoring system.

The Boeing test monitoring system for the SiGe Electronic Module.



SiGe Electronic Module located on the back of the TPS (tile) panel.

- X-Ray of SiGe module after Acoustics and Thermal testing.
- Testing and Oven Heat Soak at 260^{o}C for about 18 hours.
- Module was still functional. X-ray shows that there is no sign of degradation to the module.

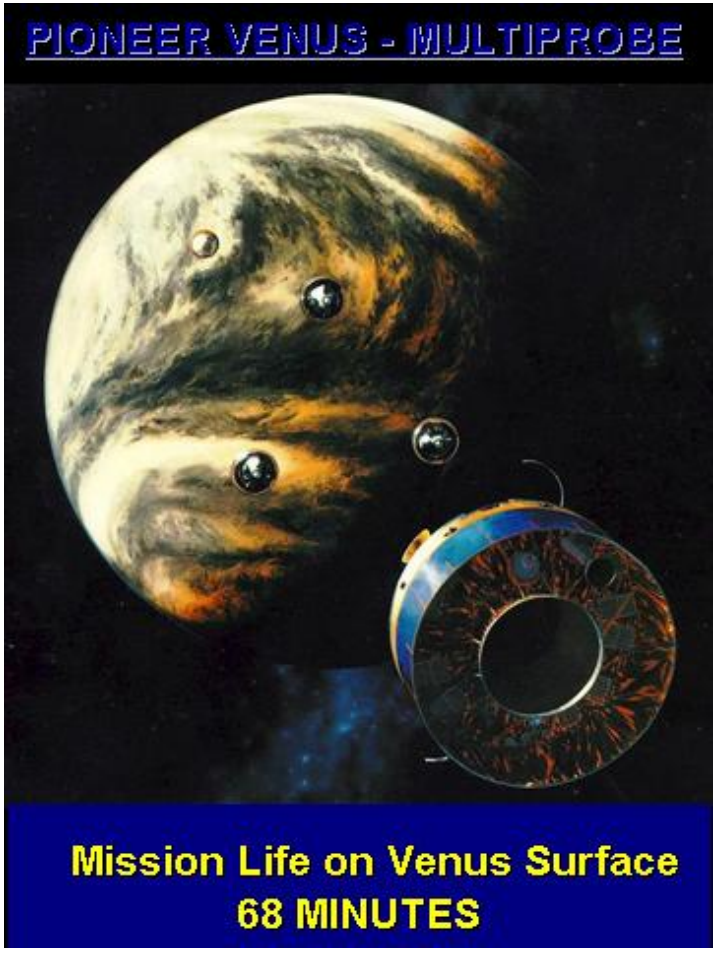


Venus Environment:
480^{o} C and 90 Bars Pressure at Surface

Venus Missions from the 1970s and 80s lasted under 2 hours on the Venus surface (electronics isolated in dewar from extreme heat).

NASA's "Venus Mobile Explorer" mission is required to have mission lifetime of 90 days on the Venus Surface.

Gallium Nitride (GaN) electronics could meet this 90 day mission requirement.



Illustrative concepts of future missions close to the Venus surface

This 90-day Venus Mission will be either a Lander/Rover or an Aerobot (pictured)

Aerobot Concept for Venus Mobile Explorer

This long-lived in-situ Flagship class mission would provide aerial mobility close to the surface (approximately 10 kilometers above the surface) using metallic bellows to tolerate the extreme environment of Venus, where the temperature reaches 460 degrees Celsius, and the pressure is up to 90 bars, and the super critical carbon dioxide atmosphere is highly corrosive.

High Temperature Electronics Technologies

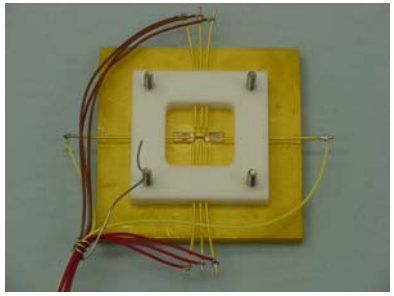
Candidate Technologies for High Temperature Operation (and Maturity Level)

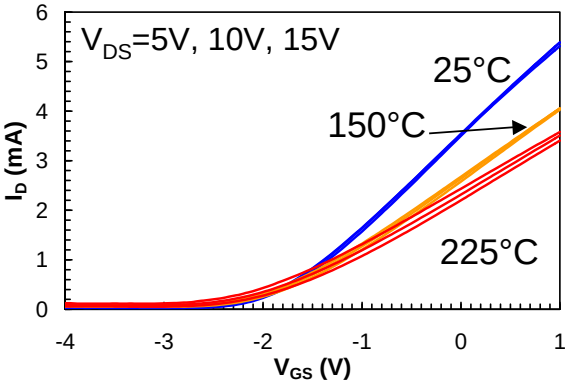
Technology	Temperature	Radiation tolerance	Integration level	Maturity
Silicon ~1.1eV	~125°C	Needs hardening	High	Very mature
SOI / SiGe ~1.1eV	~225°C (goal: 260°C)	Hard	Med-high	Mature / Maturing
SiC ~3.2eV (4H)	>300°C (goal: 600°C)	Hard	Discrete power	Emerging
GaN ~3.4eV	>350°C (goal: 500°C)	Very hard	Medium	Emerging

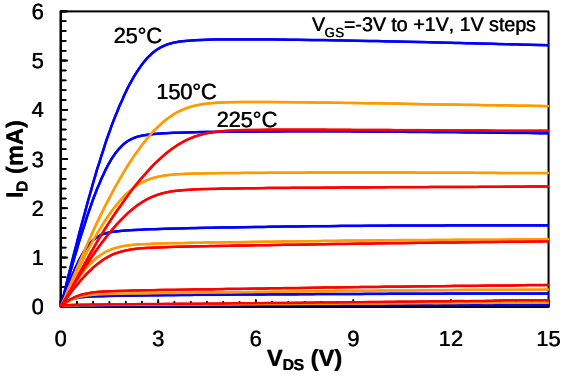
GaN ICs can provide solutions in integrated power and high temperature, high voltage, high radiation environments

Characteristic behavior of GaN technology over temperature

10μm/1μm GaN HFET Fabricated at HRL: Robust operation demonstrated to 225°C



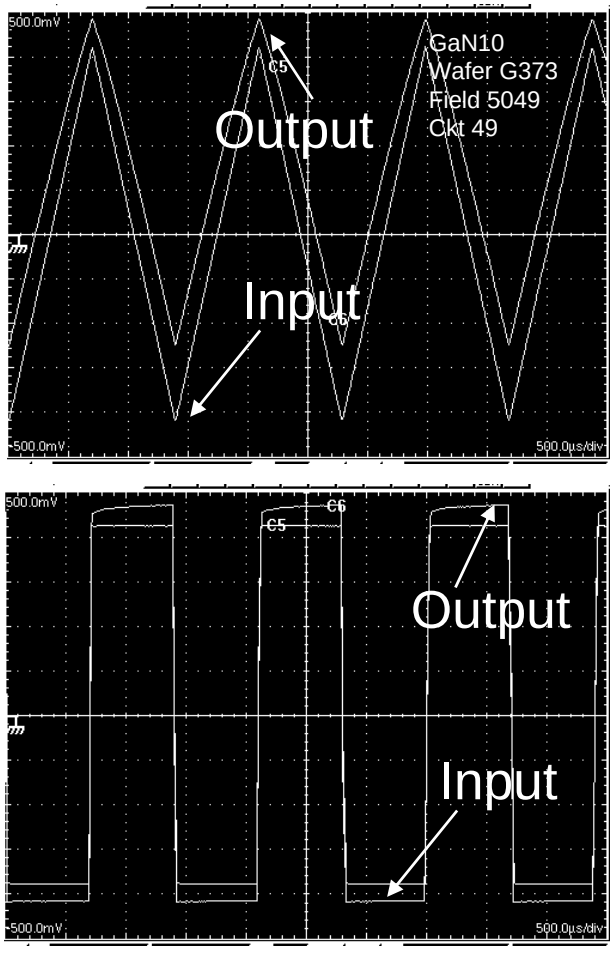




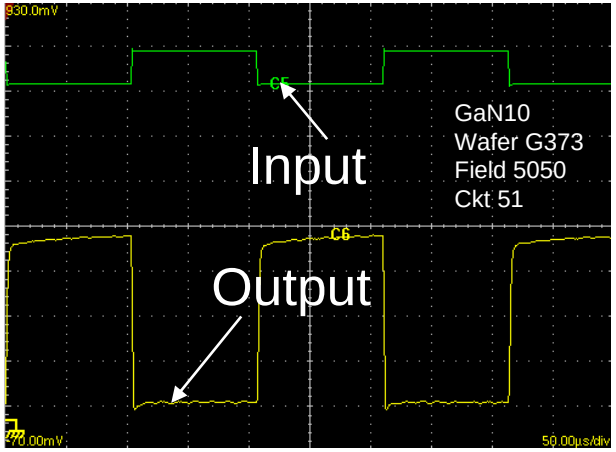
Status in 2007-2008:

- **Screened Integrated Circuits to 225°C operating temperatures**
- **HRL test fixture has capability to 300ºC, successful exploration at 375ºC**
- **Test capability at Boeing Huntington Beach, up to 500ºC, in nitrogen flow.**
- **Nominal -1.8V threshold voltage shows no sign of short channel effects**
- **Unit transconductance scales well with device size.**
- **Both on-resistance and output conductance also scale well with device size**

Illustrative examples of GaN Integrated Circuits



GaN Op-amp in unity gain and inverting gain configurations, driving 50Ω load (100mV/div)

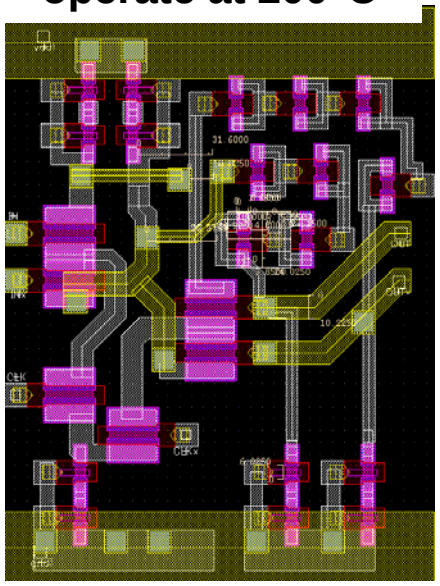


A General-purpose GaN Op-Amp Suitable for Operation in Harsh Environments

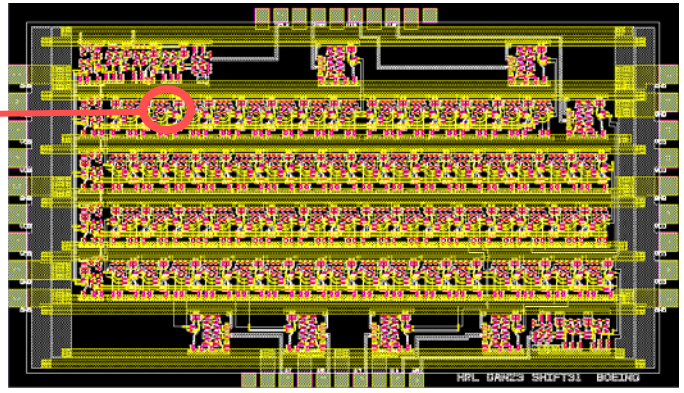
Illustrative examples of GaN Integrated Circuits

- Consists of 3 implementations of shift register
  - 4-bits (418 transistors) in a pad frame picked for packaging
  - 15-bits (1084) and 31bits (1960) with external configuration as PRBS as an option
- Copies of two different verified designs of OP-Amps from GaN18
- Provision for backside plated metal for high-temperature packages

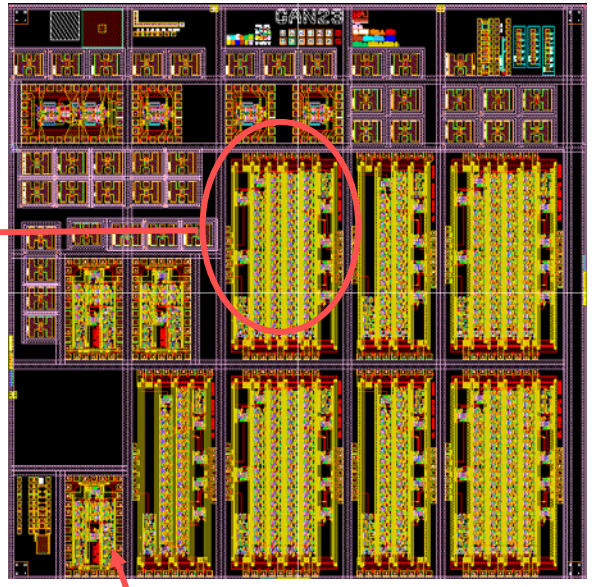
Latch designed to operate at 200ºC



31 bit shift register



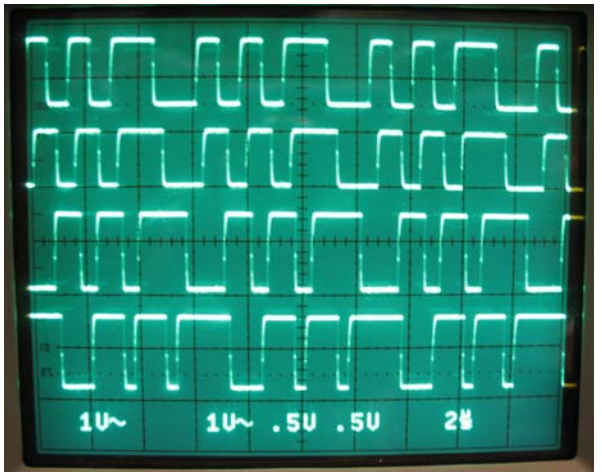
GaN23



4 bit shift register

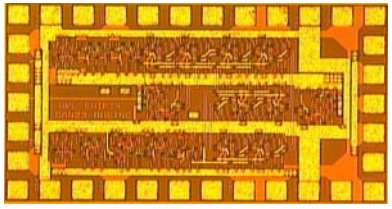
Illustrative examples of GaN Integrated Circuits

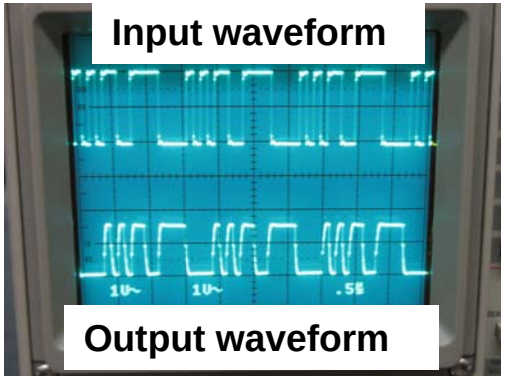
- Basic functionality screen for Shift4 done
  - Operation verified to 10MHz
  - Yield on G536 wafer is ~80%,
  - G490 (had epi-material defects) yield ~50%
- Shift31 functionality verified on G536
- Ongoing testing, to understand yield



Shift31 test result

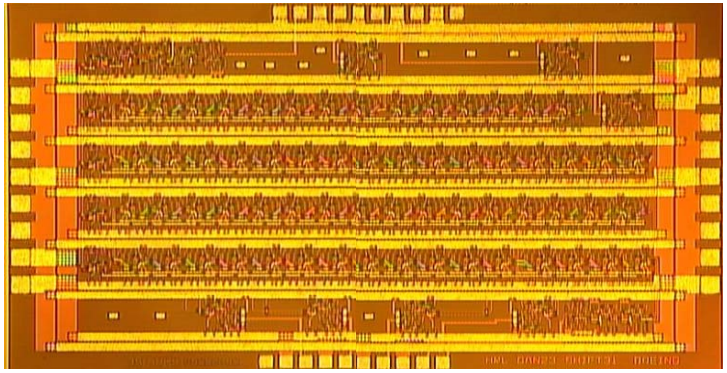
Micrograph of 4-bit shift-register



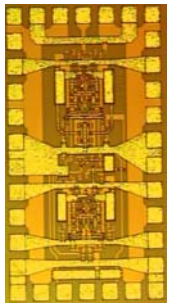


Shift4 test result

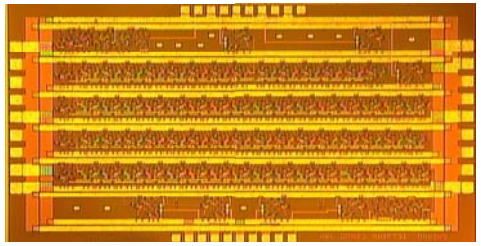
Micrograph of 31-bit shift-register



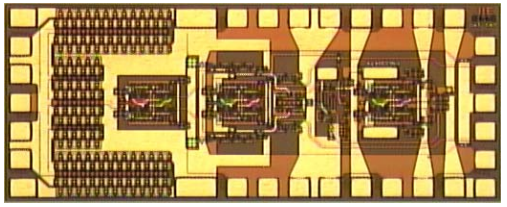
Illustrative examples of GaN Integrated Circuits (cont.)



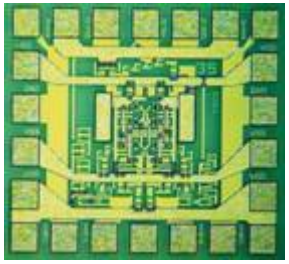
GaN Op-amps



GaN shift register

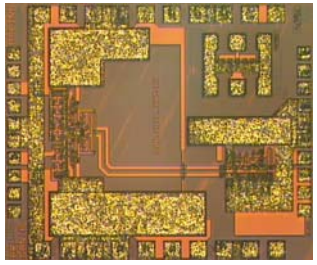


GaN Low-Dropout Voltage Regulator



GaN Voltage Reference IC

GaN switch driver IC



Demonstrating mixed-signal and power system capabilities in GaN IC technology